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(54) Multilevel Interconnect Structure

(57) The integrated device comprises, in combination: a first conductive region (6); a first insulating region (7) of dielectric material, covering the first conductive region; a first through region (15) of electrically conductive material, extending inside the first insulating region (7), and in direct electrical contact with the first conductive region (6); a second conductive region (10a), arranged above the first insulating region (7), in a position not aligned and not in contact with the first through region (15); a second insulating region (9) of dielectric material, covering the second conductive region (10a); a second through region (21) of electrically conductive material, extending inside the second insulating region (9) as far as the first through region (15), aligned and in direct electrical contact with the first through region; and a third conductive region (11a), arranged above the second insulating region (9), aligned and in direct electrical contact with the second through region (21).

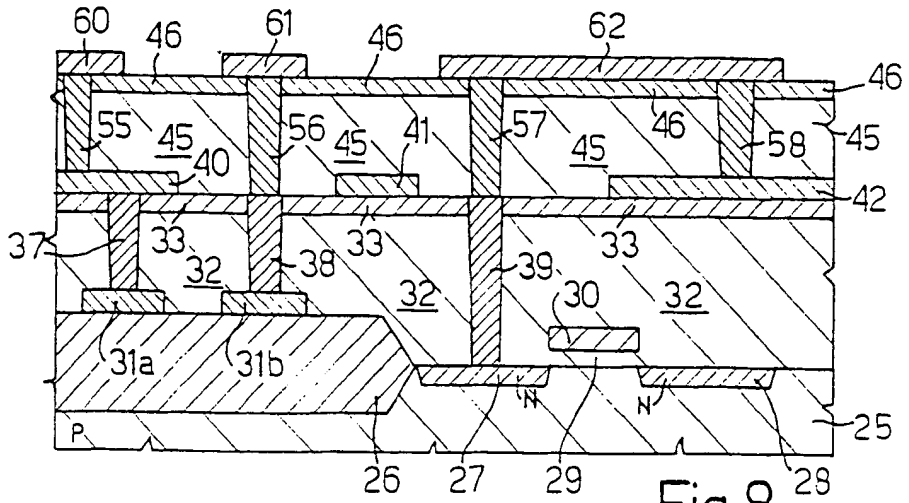

Fig.8

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Description

[0001] The present invention relates to an integrated semiconductor device having a plurality of connection levels, and a manufacturing method thereof.

[0002] As known, the integration of semiconductor devices is always and always increasing, because of the progresses in the semiconductor technology. In particular, the availability of a plurality of metal layers for interconnections has been decisive in making the signal routing more compact.

[0003] In devices having a plurality of connection levels (layers of metal or another conductive material), electrical connections exist between connection regions formed in successive connection levels, and between connection levels formed in the first connection level and regions integrated in the device substrate; these connections are formed by through regions (plugs or contacts) extending through the insulating material separating the various connection levels from one another, and from the integrated regions of the device. In addition, connections are sometimes present between connection regions belonging to non-consecutive connection levels, for example between an (N-1)-th metal layer and an (N+1)-th metal layer, or between integrated regions and connection regions that do not belong to the first metal level. In this case, now, it is necessary to form intermediate regions or islands in the intermediate connection layer (for example the N-th metal layer).

[0004] An example of connection between a connection region formed in the third level (third metal layer) and a connection region formed in the first level (first metal layer) is shown in figures 1a and 1b, which show respectively a top plan view and a cross-section of a device 1. The device 1 comprises a substrate 3 of a first conductivity type (for example P), accommodating an integrated region 4 of a second conductivity type (for example N). On substrate 1 there extend in succession a first dielectric layer 5, a first metal level 6, a second dielectric layer 7, a second metal level 10, a third dielectric layer 9, and a third metal level 11.

[0005] The first metal layer 6 comprises a first connection region 6a; the second metal layer 10 comprises second connection regions 10a, and the third metal layer 11 comprises a third connection region 11a. The first connection region 6a is connected to the integrated region 4 by a contact 12, which extends through the first dielectric layer 5; in addition, the first connection region 6a is connected to the third connection region 11a by an intermediate region or "island" 10b, which is formed in the second metal level 10. The intermediate island 10b is connected to the first connection region 6a by a first plug 15 passing through the second dielectric layer 7, and it is connected to the third connection region 11a by a second plug 16 passing through the third dielectric layer 9.

[0006] The manufacture of the intermediate island 10b involves a certain bulk, since it is necessary to comply with rules regarding the width of the intermediate island (which is therefore wider than plugs 15, 16), and the minimum distance from the regions (connection regions 10b) formed on the same metal level. It is apparent that when different connections must be provided between connection and/or integrated regions belonging to non-adjacent levels, this results in a considerable spatial dimension. In addition, sometimes, the space required by the intermediate islands does not allow the device layout to be optimized. This is the case for example of non-volatile EPROM, EEPROM and flash-EEPROM memories, wherein it is required to connect all, or a large number, of polysilicon control gate regions on the first metal level ("word line strap"), and the drain regions on the same bit line on the second metal level to reduce the capacitive connection between the second metal level and the substrate, and thus the parasitic capacities.

[0007] The object of the invention is thus to provide a solution allowing a reduction in the space necessary for connecting two connection regions (or a connection region and an integrated region of the device), arranged on non-consecutive levels.

[0008] According to the present invention, an integrated semiconductor device having a plurality of connections levels and a manufacturing method thereof are provided, as defined in claims 1 and 10 respectively.

[0009] To help understanding of the present invention, preferred embodiments are now described, purely by way of non-limiting example, with reference to the attached drawings, wherein:

- figure 1a shows a top plan view of a known device;
- figure 1b shows a cross-section through the known device of figure 1;
- figure 2a shows a top plan view of a device according to the invention;
- figure 2b shows a cross-section through the device of figure 2a;
- figures 3-8 show cross-sections through a second embodiment relating to a memory device, in successive manufacturing steps; and
- figure 9 shows a cross-section through a third embodiment of the invention.

[0010] In figures 2a, 2b, the parts of the integrated device 20 in common with the known device 1 of figures 1a and 1b, are shown with the same reference numbers, and will not be described again.

[0011] In detail, in device 20, the intermediate island 10b is not present, and the second plug passing through the third dielectric layer 9, here indicated at 21, extends as far as the first plug 15, and is in direct contact with the latter for the connection to the first connection region 6a.

[0012] As can be seen, plugs 15, 21 have cross dimensions that are substantially constant and equal to each other, and the entire connection structure between

the third connection region 11a and the first connection region 6a has a much smaller dimension than the solution of figure 1b, because of the lack of the intermediate island 12, which, according to the existing integration rules, should be much wider than the plugs, as already stated.

[0013] In general, the cross dimensions of plugs 15, 21, and the provided tolerances are such as to ensure electrical continuity between the plugs 15, 21, even in case of misalignment of the etching masks of the second and third dielectric layers 7, 9; it will be appreciated that the contact area is reduced as the misalignment increases, however the metal forming the plugs 15, 21 guarantees the electrical continuity. Of course, the dimensions must be designed so that any misalignments do not jeopardize the electrical insulation between the plug 21 and the second connection regions 10a; the distance required to guarantee this insulation is however shorter than the dimensions obtainable photolithographically, such that in any case, elimination of the intermediate islands involves reduction of the dimensions.

[0014] To manufacture the device 20, during shaping of the second metal level 10, the intermediate island 10b is not formed, and etching of the third dielectric layer 9 is prolonged such as to remove the dielectric layer also to a depth equivalent to the thickness of the second metal level 10, such as to reach the first plug 15. Although etching of the dielectric layer 9 is carried out for a greater thickness than in case of device 1 (figures 1a, 1b), this is not a problem, since the selectivity of etching between the dielectric material and the metal material is high, and it is thus possible to prolong etching without damaging the connection regions where connection apertures are simultaneously formed.

[0015] Advantageously, to avoid the lower dielectric layer to be damaged (in this specific case layer 7), in case of misalignment of the etching masks of the third dielectric layer 9 with respect to the second dielectric layer 7, at least the second dielectric layer can be formed from two superimposed layers with different etching characteristics, such that they can be selectively removed. In this case, etching of the third dielectric layer 9 stops automatically at the second dielectric layer 7.

[0016] An embodiment of a process using two dielectric layers, as previously described, for electrically connecting a drain region of a floating gate, non-volatile memory element to the second metal level, is now described with reference to figures 3-8.

[0017] In detail, the manufacturing method starts with conventional steps typical of a MOS process, as far as depositing and planarizing a first insulating layer of dielectric material; in the example shown in figure 3, a structure can be seen comprising a substrate 25 of P-type, a field oxide region 26; a drain region 27 and a source region 28 of N-type, obtained by selectively introducing doping ion species the substrate 25; a gate oxide region 29 arranged on substrate 25; a gate region 30; conductive polysilicon regions 31a, 31b on field oxide region 26, and a first insulating layer 32, typically of silicon oxide SiO_2, with a thickness of for example, approximately 500 nm. First insulating layer 32 can optionally be formed in two different steps, for example by depositing TEOS (TetraEthylOrthoSilicate), and/or SOG (Spin On Glass), and/or BPSG (Boron Phosphorous Silicon Glass). Preferably, the first insulating layer 32 is planarized through a reflow step, and then through CMP (Chemical Mechanical Polishing), to guarantee optimum planarization of the surface.

[0018] Subsequently, on the first insulating layer 32, already planarized, a first stop layer 33 of dielectric material is deposited, for example silicon nitride, with a thickness of, for example, approximately 50 nm; a contact etching mask is formed, and contacts are opened through the first stop layer 33 and the first insulating layer 32, using first an etching solution permitting removal of silicon nitride of the first stop layer 33, and then an etching solution removing silicon oxide of the first insulating layer 32. After removing the contact etching mask, the structure of figure 4 is obtained, wherein apertures 34, 35 extend as far as conductive polysilicon regions 31a, 31b, and an aperture 36 extends as far as drain region 27.

[0019] Apertures 34, 35, 36 are then filled with conductive material, and typically tungsten; for this purpose, after any steps of cleaning and depositing a barrier layer, for example titanium nitride (not shown), a filling layer is deposited, and an etch-back step is carried out, for removing without mask the filling layer above the first stop layer 33. Consequently, the filling material remains only inside apertures 34, 35, 36, forming plugs 37, 38, 39, as shown in figure 5.

[0020] Subsequently a first metal material layer (for example aluminium or copper) is deposited; the first metal material layer, forming the first metal level, is then defined to form connection regions, according to the design; in particular, in figure 6, three connection regions 40, 41, 42 are shown, whereof connection region 40 is in electrical contact with plug 37. Intermediate islands are not formed in this step.

[0021] A second insulating layer 45, typically of SiO_2, is then formed, similarly to the first insulating layer 32; the second insulating layer 45 is planarized by reflow and CPM; and a second stop layer 46, typically silicon nitride, is then deposited. Then, using a second mask and double RIE (Reactive Ion Etching) with two different chemicals, apertures 50, 51, 52 and 53 are formed, which pass through second stop layer 46 and second insulating layer 45. In detail, as shown in figure 7, aperture 50 ends at the connection region 40 of the first metal level; aperture 51 ends at plug 38; aperture 52 ends at plug 39; and aperture 53 ends at connection region 42 of the first metal level.

[0022] Subsequently, and similarly to the previous case, apertures 50-53 are filled with conductive material, and typically tungsten, after any steps for cleaning and depositing a barrier layer, by depositing a filling lay-

er and etching back. Thus, on completion, inside apertures 50-53, plugs 55, 56, 57 and 58 are formed, as shown in figure 3. In particular, plug 56 is aligned and in direct electrical contact with plug 38, and plug 57 is aligned and in direct electrical contact with plug 39.

[0023] A second metal material layer (for example aluminium or copper) is then deposited and defined, forming the second metal level; three connection regions 60, 61, 62 are then formed, whereof connection region 60 is in electrical contact with plug 55; connection region 61 is in electrical contact with plug 56; and connection region 62 is in electrical contact both with plug 57 and plug 58. Thereby, connection region 61 is in electrical contact with connection region 31b, and connection region 62 is in electrical contact with drain region 27, without requiring intermediate islands on the first metal level. This allows, inter alia, to arrange connection region 41 as shown, whereas forming intermediate islands between plugs 56, 38 on the one hand, and 57, 39 on the other hand, is not possible, or would require greater space between connection regions 61 and 62.

[0024] Figure 9 shows a variant of figure 3, wherein connection regions 40 and 42 of the first metal level are protected from over-etching when forming stacked plugs 56, 57. In fact, as already stated, over-etching which is necessary to form the plugs (here 56, 57) in general does not damage significantly the connection regions (here 40, 42), where the apertures (in this case 50, 53) are formed, by virtue of selectivity of metal with respect to connection region etching. However, to be certain of preventing damage to the metal in all conditions, it is possible to protect these connection regions by depositing first the stop layer and then the inter-metallic dielectric layer, which prevents breakdown. This solution is shown in figure 9, wherein the parts common to figure 8 have the same reference numbers. In detail, in this case, a second stop layer 46a is disposed directly above the first metal level, including connection regions 40-42, and is open only at the plugs 56-58; the second dielectric layer 45a extends above. Consequently, first stop layer 33 is no longer necessary; optionally, and similarly to layers 45a, 46a, below the first dielectric layer 32 of oxide, the nitride stop layer can be arranged, in a manner not shown.

[0025] For manufacturing the device of figure 9, after the first level connection regions 40-41 have been defined, first the second stop layer 46a (for example of nitride), and then the second dielectric layer 45a (for example of oxide) are deposited; subsequently the apertures 50-53 are formed by carrying out initial RIE with a first etching chemical, to selectively remove oxide of the second dielectric layer 45a; this step includes an over-etching as necessary in order to excavate the greater depth at the plugs 38, 39, and is stopped automatically at the second stop layer 46a; a second RIE step is then carried out with a second etching chemical, in order to selectively remove nitride of the second stop layer 46a, for a time correlated to the thickness of second stop layer 46a. Thereby, the second connection regions 40, 42 are protected by the second stop layer 46a during over-etching necessary to form plugs 56, 57.

[0026] The advantages of the described device and the method are the following. First, the bulk for connecting connection and/or integrated regions arranged on non-adjacent levels is reduced. In addition, the described method comprises only known process steps and can therefore be implemented using equipments commonly used in the microelectronics industry. The method is simple and reliable, and does not create problems of implementation. If a double dielectric layer is used, as shown in the embodiment of figures 3-8, it is possible to carry out slight over-etching of the upper dielectric layer (the second insulating layer 45, in the example), thus ensuring that the apertures (the apertures 50-53, in the example) are formed correctly, since even if the etching masks are misaligned, etching of an upper insulating layer (45 in the example) stops automatically at the underlying stop layer (the first stop layer 33, in the example illustrated).

[0027] Finally, it is apparent that many modifications and variants can be made to the device and method described and illustrated here, all of which come within the scope of the invention, as defined in the attached claims. In particular, it is emphasised that the described structure can be applied to devices of a different type, as long as they comprise at least two metal levels. In addition, in general, it allows connection between a metal level N-1 and a metal level N+1, thus eliminating the intermediate islands on metal level N. The described solution can also be replicated on additional, upper metal levels such as to obtain a plurality of apertures and plugs stacked one on another, for as much as 3 or 4 levels. Any method for planarizing the insulating layer can be used, for example may not include CMP; the dielectric stop layer can be provided on only some levels or on none of them, if the manufacturing method used guarantees a high level of alignment of the masks.

Claims

1. An integrated semiconductor device having a plurality of connection levels, characterised, in combination, by:

   - a first conductive region (6; 27, 31b) inside or above a substrate (3; 25) of semiconductor material;
   - a first insulating region (7; 32, 33) of dielectric material, covering said first conductive region;
   - a first through region (15; 39, 38) of electrically conductive material, extending inside said first insulating region (7; 32, 33), and in direct electrical contact with said first conductive region (6; 27, 31b);
   - a second conductive region (10a; 40, 41, 42),

arranged above said first insulating region (7; 32, 33), in a position not aligned and not in contact with said first through region (15; 39, 38);

- a second insulating region (9; 45, 46) of dielectric material, covering said second conductive region (10a; 40, 41, 42);
- a second through region (21; 57, 56) of electrically conductive material, extending inside said second insulating region (9; 45, 46), as far as said first through region (15; 39, 38), aligned and in direct electrical contact with said first through region; and
- a third conductive region (11a; 62, 61), arranged above said second insulating regions (9; 45, 46), and aligned and in direct electrical contact with said second through region (21; 57, 56).

2. A device according to claim 1, characterised in that said first and second through regions (15 and 21; 39, 38 and 57, 56) have a substantially constant cross-sectional dimension.

3. A device according to claim 2, characterised in that said first and second through regions (15 and 21; 39, 38 and 57, 56) have a substantially equal cross-sectional dimension.

4. A device according to any one of claims 1-3, characterised in that said first conductive region (27) is of semiconductor material, and is accommodated in said substrate (25).

5. A device according to any one of claims 1-3, characterised in that said first conductive region (6) is of metal material, a third insulating region (5) extends above said substrate (25), and said first conductive region extends above said third insulating region.

6. A device according to any one of claims 1-3, characterised in that said first conductive region (31b) is of semiconductor material, a fourth insulating region (26) extends above said substrate (25), and said first conductive region extends above said fourth insulating region.

7. A device according to any one of claims 1-6, characterised in that said second (10a; 40, 41, 42) and said third (11a; 62, 61) conductive regions are formed from successive metal levels.

8. A device according to any one of claims 1-7, characterised in that at least one of said first (32, 33) and second (45, 45a, 46, 46a) insulating regions comprise a first insulating layer (32, 45, 46a) of a first dielectric material, and a second insulating layer (33, 46, 45a) of a second dielectric material, which are superimposed on each other.

9. A device according to claim 8, characterised in that said first dielectric material comprises silicon oxide, and said second dielectric material comprises silicon nitride.

10. A method for manufacturing an integrated semiconductor device, comprising a plurality of connection levels, characterised in that it comprises, in combination, the steps of:

- forming a first conductive region (6; 27, 31b) inside or above a substrate (3; 25) of semiconductor material;
- forming a first insulating region (7; 32, 33) of dielectric material above said first conductive region;
- forming a first through region (15; 39, 38) of electrically conductive material inside said first insulating region (7; 32, 33), and in direct electrical contact with said first conductive region (6; 27, 31b);
- forming a second conductive region (10a; 40, 41, 42) above said first insulating region (7; 32, 33), in a position not aligned and not in contact with said first through region (15; 39, 38);
- forming a second insulating region (9; 45, 46) of dielectric material, covering said second conductive region (10a; 40, 41, 42);
- forming, inside said second insulating region (9; 45, 46), a second through region (21; 57, 56) of electrically conductive material, extending as far as said first through region (15; 39, 38), aligned and in direct electrical contact with said first through region; and
- forming, above said second insulating region (9; 45, 46), a third conductive region (11a; 62, 61) aligned and in direct electrical contact with said second through region (21; 57, 56).

11. A method according to claim 10, characterised in that said first (15; 39, 38) and second (21; 57, 56) through regions have a substantially constant cross-sectional dimension.

12. A method according to claim 10 or claim 11, characterised in that said step of forming said first conductive regions (27) comprises the step of introducing doping ion species inside said substrate (25).

13. A method according to any one of claims 10-12, characterised in that said first conductive region (6) is of metal material, a third insulating region (5) extends above said substrate (25), and said first conductive region extends above said third insulating region.

14. A method according to any one of claims 10-13, characterised in that said second (10a; 40, 41, 42)

and said third (11a; 62, 61) conductive regions are formed in successive metal levels.

15. A method according to any one of claims 10-14, characterised in that said first insulating region (32, 33) comprises a first insulating layer (32) of a first dielectric material, and a second insulating layer (33) of a second dielectric material, superimposed on each other, in that said step of forming said first through region (39, 38) comprises, in succession, the steps of etching said second dielectric material (33) with first etching parameters, etching said first dielectric material (32) with second etching parameters, thereby forming a through aperture (36, 35) in said first insulating region, and to fill said through aperture with said electrically conductive material.

16. A method according to claim 15, characterised in that said first dielectric material comprises silicon oxide, and said second dielectric material comprises silicon nitride.

17. A method according to claim 15, characterised in that said first dielectric material comprises silicon nitride, and said second dielectric material comprises silicon oxide.

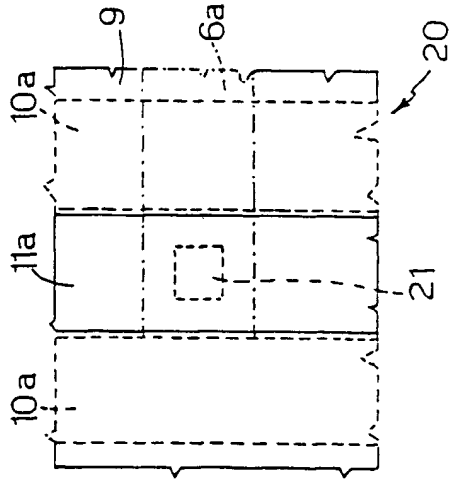

Fig.2a

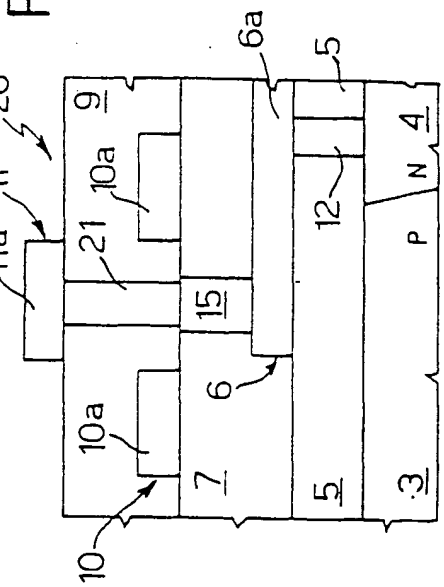

Fig.2b

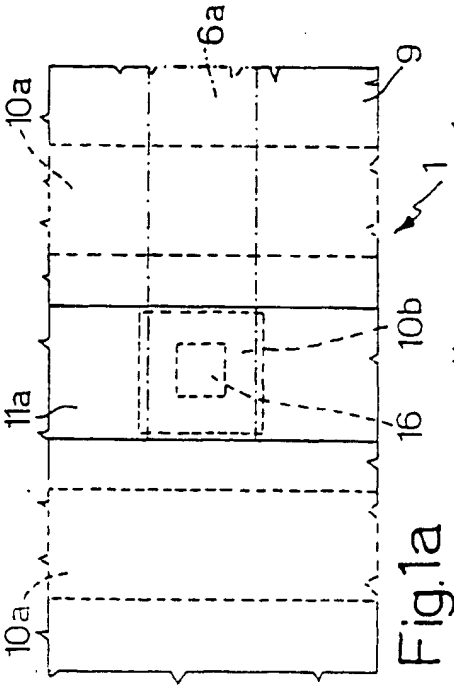

Fig.1a

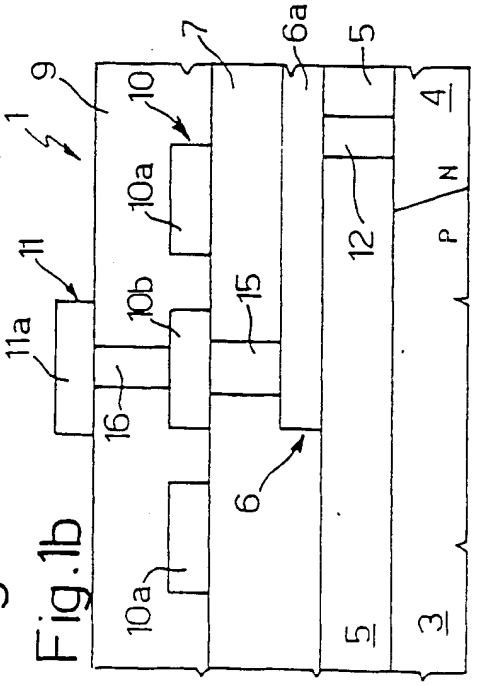

Fig.1b

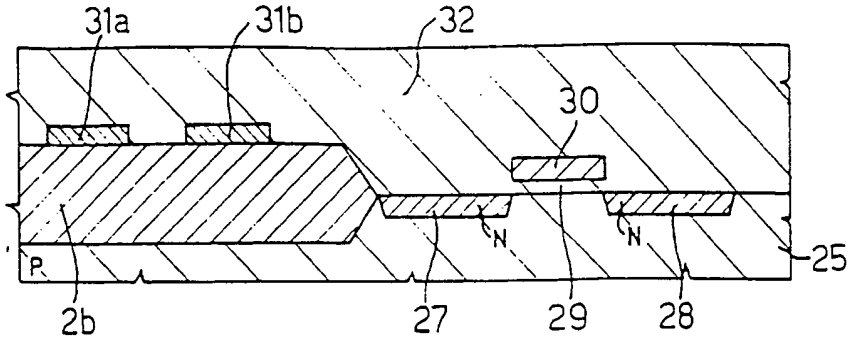

Fig.3

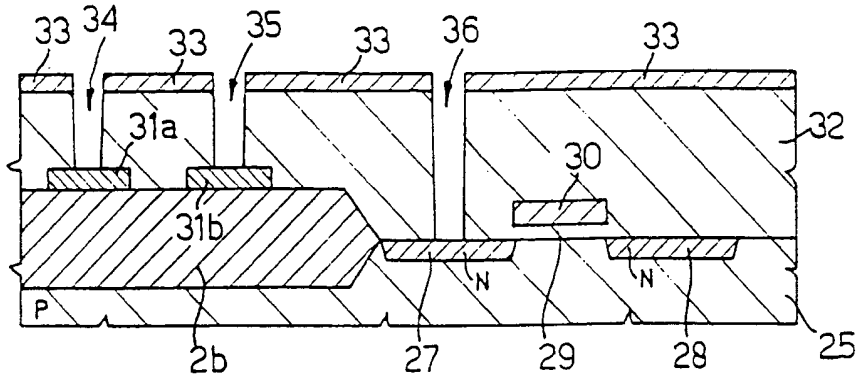

Fig.4

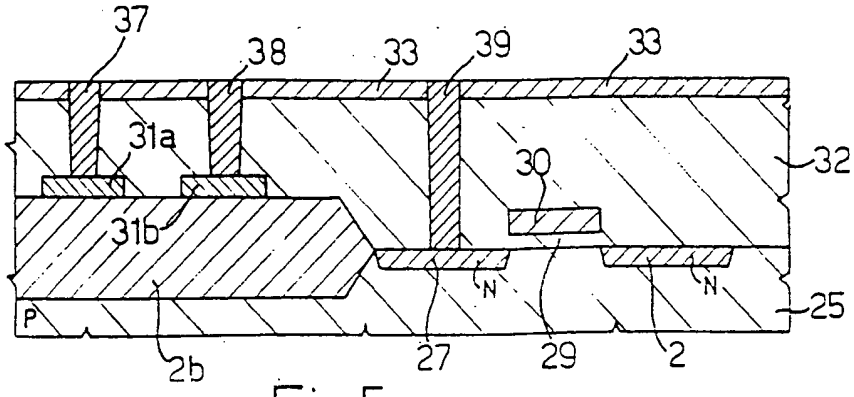

Fig.5

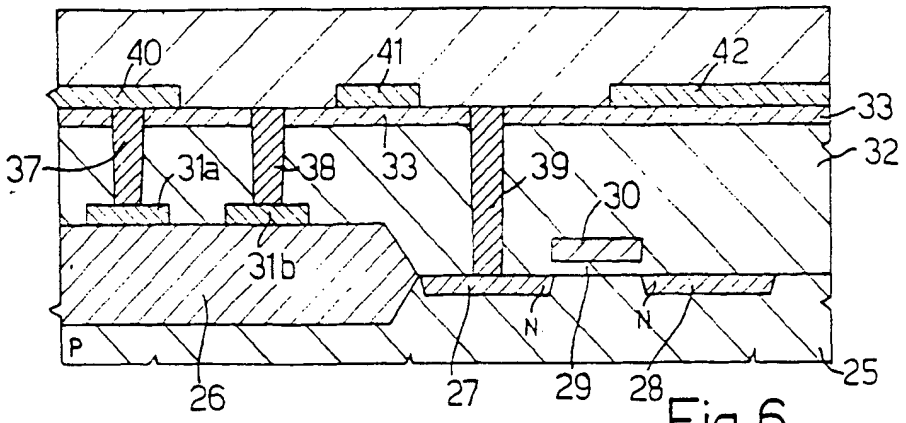

Fig.6

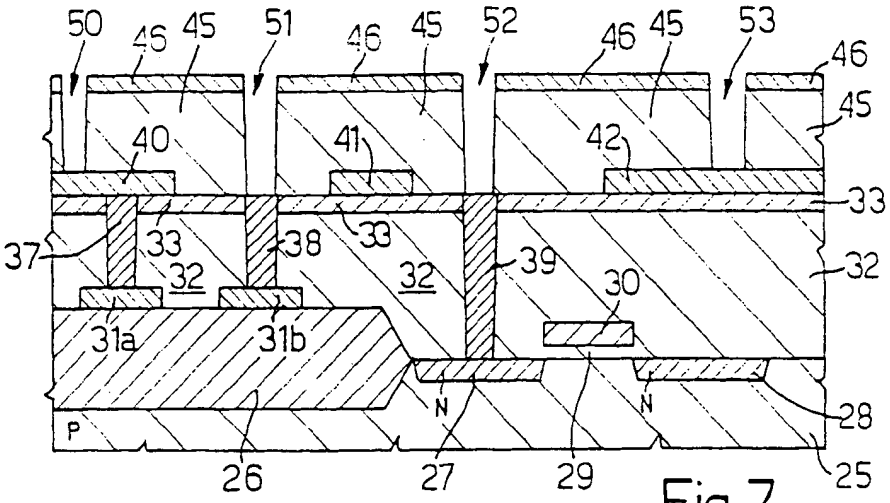

Fig.7

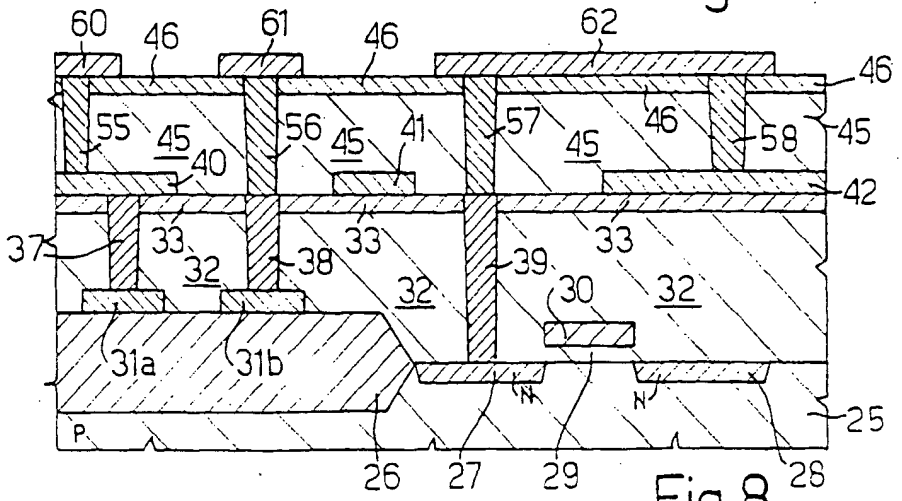

Fig.8

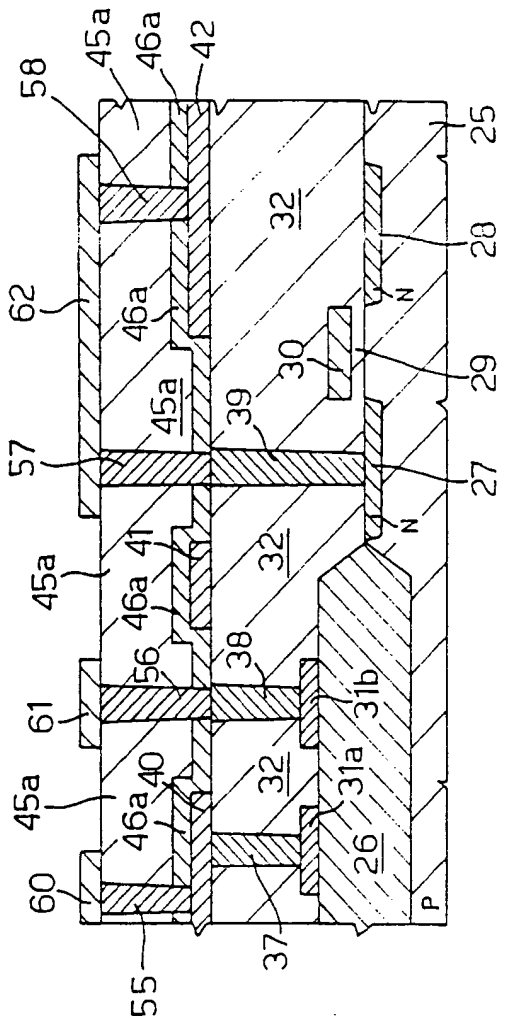
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Fig.9

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 83 0562

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X A	US 5 710 462 A (MIZUSHIMA KAZUYUKI) 20 January 1998 * column 1, line 34 - column 2, line 56; figure 1C * * column 5, line 60 - column 8, line 5; figure 3H *	1-3,7, 10,11,14 5,8,15	H01L23/522 H01L21/768
A	WO 97 11488 A (ADVANCED MICRO DEVICES INC) 27 March 1997 * figures 2,3 *	1,10	
A	FR 2 754 391 A (SGS THOMSON MICROELECTRONICS) 10 April 1998 * figures 2,3 *	1,10	
A	US 5 328 553 A (POON STEPHEN S) 12 July 1994 * figure 6 *	1-3,10	
A	US 5 717 251 A (HAYASHI YOSHIHIRO ET AL) 10 February 1998 * figure 10 *	1,10	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	3 March 1999	Königstein, C

CATEGORY OF CITED DOCUMENTS

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